1. A method of making a bit selectable device having nanotube memory elements, comprising:

providing a structure having at least two transistors, each with a drain and a source with a defined channel region therebetween, each transistor further including a gate over said channel;

forming a trench between one of the source and drain of a first transistor and one of the source and drain of a second transistor;

forming an electrical communication path in the trench between one of the source and drain of a first transistor and one of the source and drain of a second transistor;

providing a defined pattern of nanotube fabric over at least a horizontal portion of the structure and extending into the trench;

providing an electrode in the trench;

suspending defined pattern of nanotube fabric so that at least a portion is vertically suspended in spaced relation to the vertical walls of the trench and positioned so that the vertically suspended defined pattern of nanotube fabric is electromechanically deflectable into electrical communication with one of the drain and source of a first transistor and one of the source and drain of a second transistor.

2. The method of claim 1 wherein the providing of a defined pattern of nanotube fabric includes the application of pre-formed nanotubes to create a layer of nanotubes.

3. The method of claim 2 wherein the layer is substantially a monolayer of nanotubes.

4. The method of claim 2 wherein the layer is a highly porous fabric of nanotubes.

5. The method of claim 2 wherein the layer of nanotubes is a conformal fabric of nanotubes.

6. The method of claim 2 wherein the nanotubes are single walled carbon nanotubes.

7. The method of claim 1 wherein the suspended length of nanotube fabric has an extent that is sub-lithographic-critical-dimension.